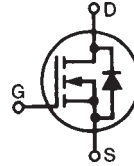


# PolarHV™ HiPerFET Power MOSFET

IXFA 16N50P  
IXFH 16N50P  
IXFP 16N50P

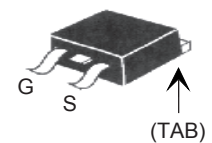
$V_{DSS} = 500 \text{ V}$   
 $I_{D25} = 16 \text{ A}$   
 $R_{DS(on)} \leq 400 \text{ m}\Omega$   
 $t_{rr} \leq 200 \text{ ns}$

N-Channel Enhancement Mode  
Avalanche Rated  
Fast Intrinsic Diode

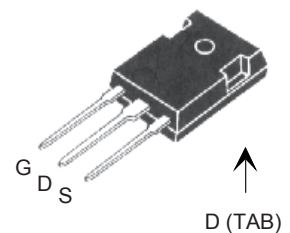


Symbol	Test Conditions	Maximum Ratings	
$V_{DSS}$	$T_J = 25^\circ\text{C}$ to $150^\circ\text{C}$	500	V
$V_{DGR}$	$T_J = 25^\circ\text{C}$ to $150^\circ\text{C}$ ; $R_{GS} = 1 \text{ M}\Omega$	500	V
$V_{GS}$	Continuous	$\pm 30$	V
$V_{GSM}$	Transient	$\pm 40$	V
$I_{D25}$	$T_C = 25^\circ\text{C}$	16	A
$I_{DM}$	$T_C = 25^\circ\text{C}$ , pulse width limited by $T_{JM}$	35	A
$I_{AR}$	$T_C = 25^\circ\text{C}$	16	A
$E_{AR}$	$T_C = 25^\circ\text{C}$	25	mJ
$E_{AS}$	$T_C = 25^\circ\text{C}$	750	mJ
$dv/dt$	$I_S \leq I_{DM}$ , $di/dt \leq 100 \text{ A}/\mu\text{s}$ , $V_{DD} \leq V_{DSS}$ , $T_J \leq 150^\circ\text{C}$ , $R_G = 10 \Omega$	10	V/ns
$P_D$	$T_C = 25^\circ\text{C}$	300	W
$T_J$		-55 ... +150	$^\circ\text{C}$
$T_{JM}$		150	$^\circ\text{C}$
$T_{stg}$		-55 ... +150	$^\circ\text{C}$
$T_L$	1.6 mm (0.062 in.) from case for 10 s	300	$^\circ\text{C}$
$T_{SOLD}$	Plastic body for 10 s soldering	260	$^\circ\text{C}$
$M_d$	Mounting torque (TO-247 & TO-220)	1.13/10	Nm/lb.in.
Weight	TO-220	4	g
	TO-263	3	g
	TO-247	5.5	g

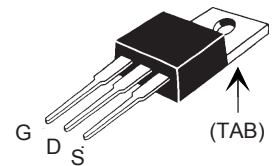
TO-263 (IXTA)



TO-247 (IXFH)



TO-220 (IXTP)



G = Gate      D = Drain  
S = Source      TAB = Drain

Symbol	Test Conditions ( $T_J = 25^\circ\text{C}$ , unless otherwise specified)	Characteristic Values		
		Min.	Typ.	Max.
$BV_{DSS}$	$V_{GS} = 0 \text{ V}$ , $I_D = 250 \mu\text{A}$	500		V
$V_{GS(th)}$	$V_{DS} = V_{GS}$ , $I_D = 2.5 \text{ mA}$	3.0		5.5 V
$I_{GSS}$	$V_{GS} = \pm 30 \text{ V}_{DC}$ , $V_{DS} = 0$			$\pm 100 \text{ nA}$
$I_{DSS}$	$V_{DS} = V_{DSS}$ , $V_{GS} = 0 \text{ V}$ , $T_J = 125^\circ\text{C}$			5 $\mu\text{A}$
				250 $\mu\text{A}$
$R_{DS(on)}$	$V_{GS} = 10 \text{ V}$ , $I_D = 0.5 I_{D25}$ Pulse test, $t \leq 300 \mu\text{s}$ , duty cycle $d \leq 2\%$			400 $\text{m}\Omega$

## Features

- † International standard packages
- † Unclamped Inductive Switching (UIS) rated
- † Low package inductance  
- easy to drive and to protect

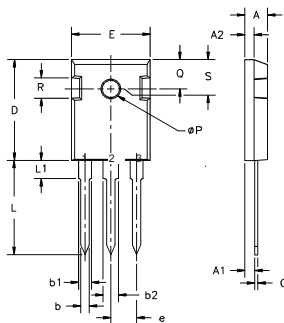
## Advantages

- † Easy to mount
- † Space savings
- † High power density

Symbol	Test Conditions	Characteristic Values		
		$(T_J = 25^\circ\text{C}, \text{ unless otherwise specified})$		
		Min.	Typ.	Max.
$g_{fs}$	$V_{DS} = 20\text{ V}; I_D = 0.5 I_{D25}, \text{ pulse test}$	8	16	S
$C_{iss}$	$V_{GS} = 0\text{ V}, V_{DS} = 25\text{ V}, f = 1\text{ MHz}$		2250	pF
$C_{oss}$			240	pF
$C_{rss}$			12	pF
$t_{d(on)}$	$V_{GS} = 10\text{ V}, V_{DS} = 0.5 V_{DSS}, I_D = I_{D25}$ $R_G = 10\ \Omega \text{ (External)}$		23	ns
$t_r$			25	ns
$t_{d(off)}$			70	ns
$t_f$			22	ns
$Q_{g(on)}$	$V_{GS} = 10\text{ V}, V_{DS} = 0.5 V_{DSS}, I_D = 0.5 I_{D25}$		43	nC
$Q_{gs}$			15	nC
$Q_{gd}$			12	nC
$R_{thJC}$				$0.42^\circ\text{C/W}$
$R_{thCS}$	(TO-220)		0.25	$^\circ\text{C/W}$
$R_{thCS}$	(TO-247)		0.21	$^\circ\text{C/W}$

Symbol	Test Conditions	Characteristic Values		
		$(T_J = 25^\circ\text{C}, \text{ unless otherwise specified})$		
		Min.	Typ.	Max.
$I_s$	$V_{GS} = 0\text{ V}$			16 A
$I_{SM}$	Repetitive			35 A
$V_{SD}$	$I_F = I_s, V_{GS} = 0\text{ V},$ Pulse test, $t \leq 300\ \mu\text{s}, \text{ duty cycle } d \leq 2\%$			1.5 V
$t_{rr}$	$I_F = 16\text{ A}, -di/dt = 100\text{ A}/\mu\text{s}$ $V_R = 100\text{ V}$		130	200 ns
$I_{RM}$			6	A
$Q_{RM}$			0.6	$\mu\text{C}$

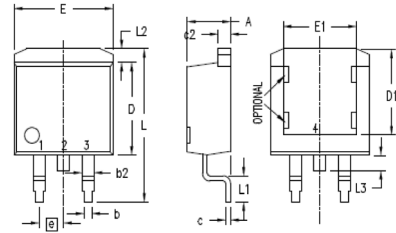
**TO-247 (IXFH) Outline**



Terminals: 1 - Gate 2 - Drain  
3 - Source Tab - Drain

Dim.	Millimeter		Inches	
	Min.	Max.	Min.	Max.
A	4.7	5.3	.185	.209
A <sub>1</sub>	2.2	2.54	.087	.102
A <sub>2</sub>	2.2	2.6	.059	.098
b	1.0	1.4	.040	.055
b <sub>1</sub>	1.65	2.13	.065	.084
b <sub>2</sub>	2.87	3.12	.113	.123
C	.4	.8	.016	.031
D	20.80	21.46	.819	.845
E	15.75	16.26	.610	.640
e	5.20	5.72	0.205	0.225
L	19.81	20.32	.780	.800
L1		4.50		.177
∅P	3.55	3.65	.140	.144
Q	5.89	6.40	0.232	0.252
R	4.32	5.49	.170	.216
S	6.15	BSC	242	BSC

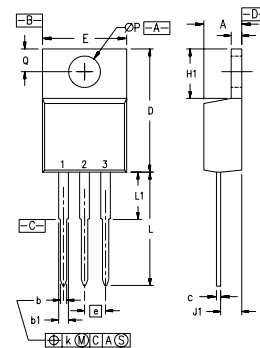
**TO-263 (IXTA) Outline**



1. GATE
  2. DRAIN (COLLECTOR)
  3. SOURCE (EMITTER)
  4. DRAIN (COLLECTOR)
- OPTIONAL  
BOTTOM SIDE

SYM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.160	.190	4.06	4.83
A <sub>1</sub>	.080	.110	2.03	2.79
b	.020	.039	0.51	0.99
b <sub>2</sub>	.045	.055	1.14	1.40
c	.016	.029	0.40	0.74
c <sub>2</sub>	.045	.055	1.14	1.40
D	.340	.380	8.64	9.65
D <sub>1</sub>	.315	.350	8.00	8.89
E	.380	.410	9.65	10.41
E <sub>1</sub>	.245	.320	6.22	8.13
e	.100 BSC		2.54 BSC	
L	.575	.625	14.61	15.88
L <sub>1</sub>	.090	.110	2.29	2.79
L <sub>2</sub>	.040	.055	1.02	1.40
L <sub>3</sub>	.050	.070	1.27	1.78
L <sub>4</sub>	0	.005	0	0.13

**TO-220 (IXTP) Outline**



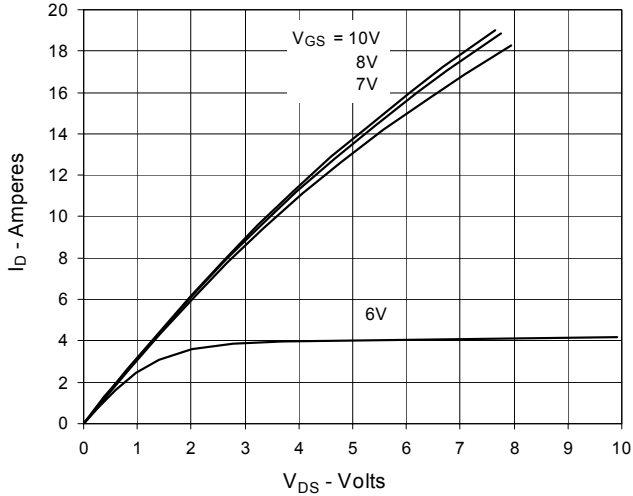
Pins: 1 - Gate 2 - Drain  
3 - Source 4 - Drain

SYM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.170	.190	4.32	4.83
b	.025	.040	0.64	1.02
b <sub>1</sub>	.045	.065	1.15	1.65
c	.014	.022	0.35	0.56
D	.580	.630	14.73	16.00
E	.390	.420	9.91	10.66
e	.100 BSC		2.54 BSC	
F	.045	.055	1.14	1.40
H1	.230	.270	5.85	6.85
J1	.090	.110	2.29	2.79
k	0	.015	0	0.38
L	.500	.550	12.70	13.97
L <sub>1</sub>	.110	.230	2.79	5.84
∅P	.139	.161	3.53	4.08
Q	.100	.125	2.54	3.18

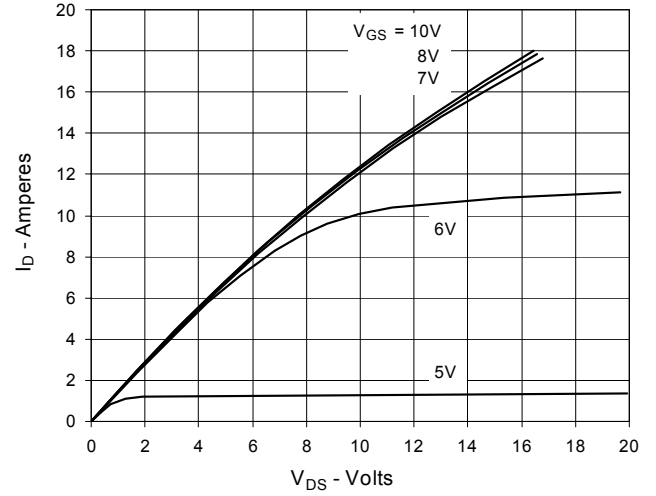
IXYS reserves the right to change limits, test conditions, and dimensions.

IXYS MOSFETs and IGBTs are covered by one or more of the following U.S. patents:	4,835,592	4,931,844	5,049,961	5,237,481	6,162,665	6,404,065 B1	6,683,344	6,727,585
	4,850,072	5,017,508	5,063,307	5,381,025	6,259,123 B1	6,534,343	6,710,405B2	6,759,692
	4,881,106	5,034,796	5,187,117	5,486,715	6,306,728 B1	6,583,505	6,710,463	6,771,478 B2

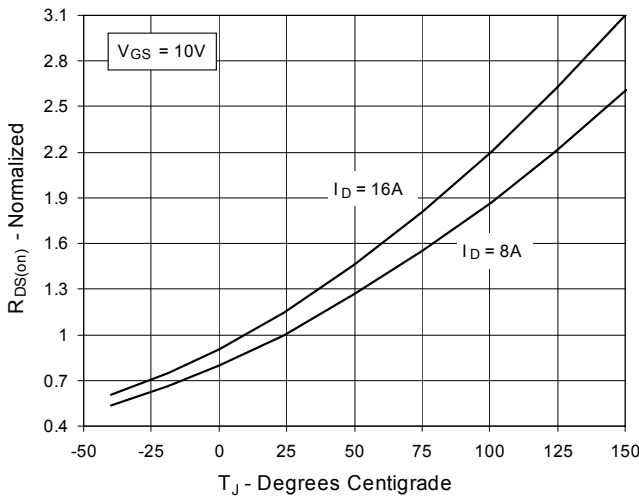
**Fig. 1. Output Characteristics @ 25°C**



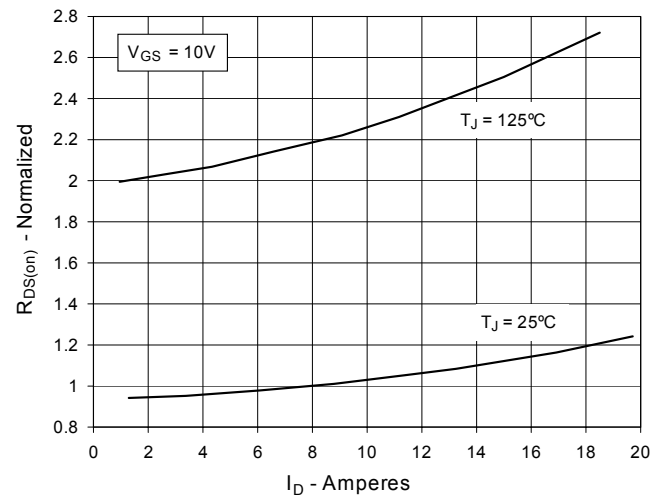
**Fig. 2. Output Characteristics @ 125°C**



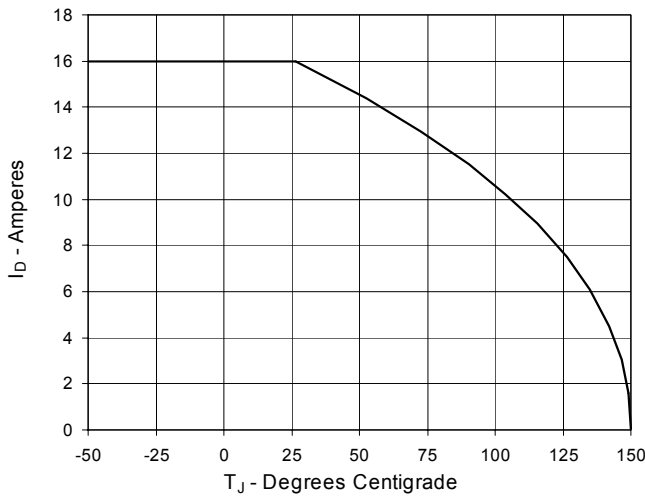
**Fig. 3.  $R_{DS(on)}$  Normalized to  $I_D = 8A$  vs. Junction Temperature**



**Fig. 4.  $R_{DS(on)}$  Normalized to  $I_D = 8A$  vs. Drain Current**



**Fig. 5. Maximum Drain Current vs. Case Temperature**



**Fig. 6. Input Admittance**

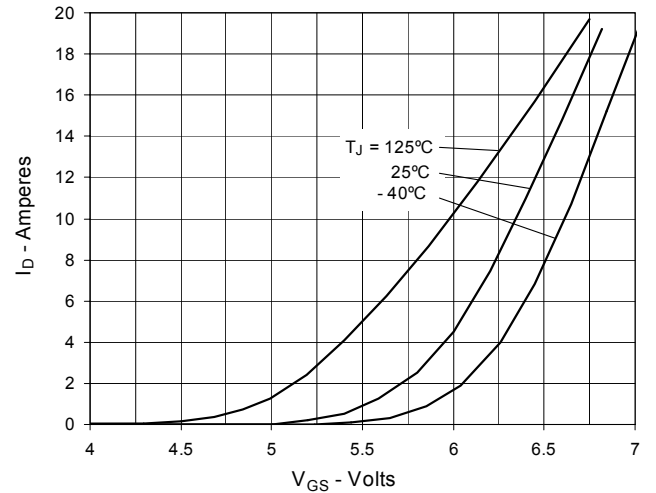


Fig. 7. Transconductance

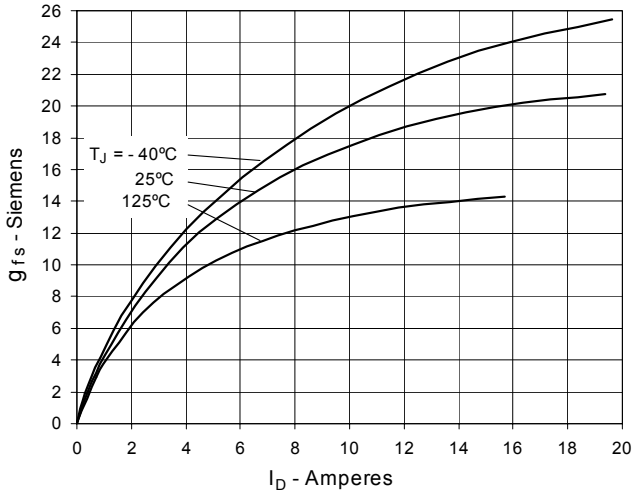


Fig. 8. Forward Voltage Drop of Intrinsic Diode

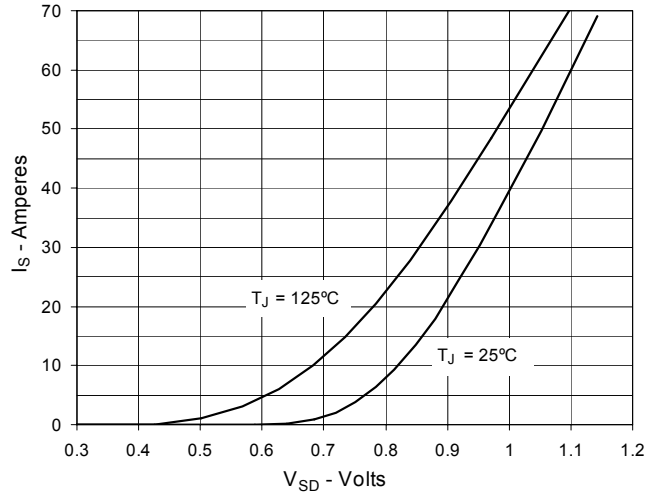


Fig. 9. Gate Charge

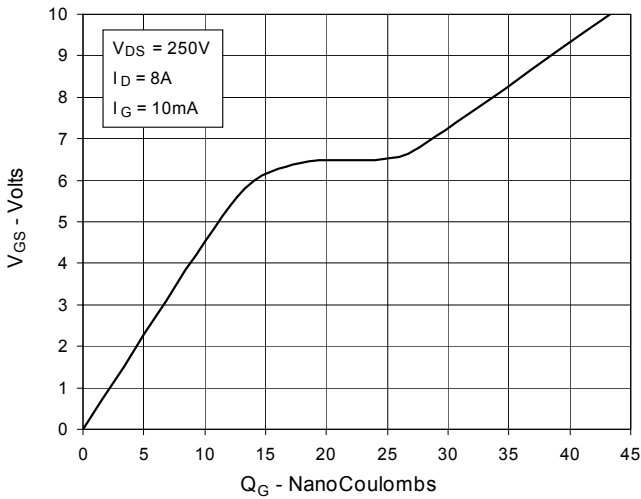


Fig. 10. Capacitance

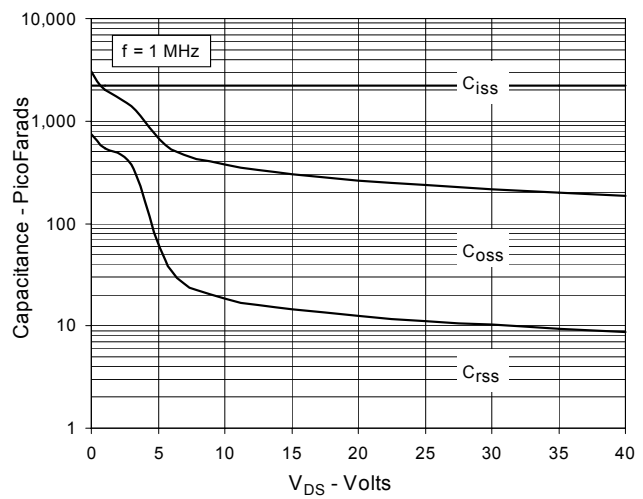


Fig. 11. Forward-Bias Safe Operating Area

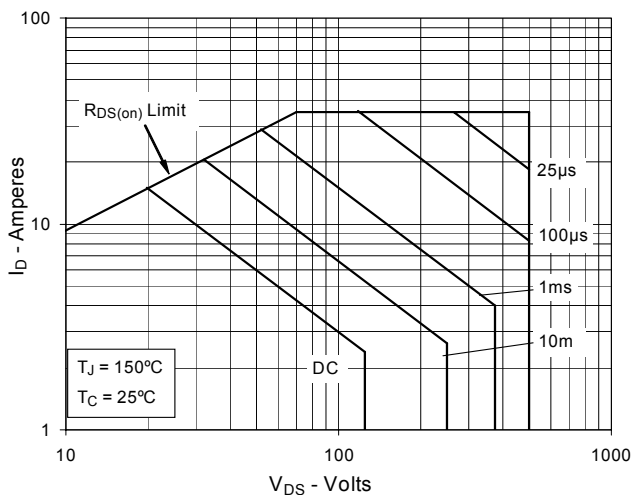


Fig. 12. Maximum Transient Thermal Resistance

